CLAIMS

WHAT IS CLAIMED:

1. A method, comprising:

forming a low-k dielectric layer over a substrate;

converting an upper portion of said low-k dielectric layer into a protective dielectric to form a sacrificial cap layer; and

patterning said sacrificial cap layer and said low-k dielectric layer.

2. The method of claim 1, wherein converting an upper portion of said low-k dielectric layer includes exposing said substrate to an oxidizing plasma ambient.

3. The method of claim 2, wherein said low-k dielectric layer comprises a silicon-based dielectric material.

4. The method of claim 1, wherein said low-k dielectric layer is formed with a thickness that exceeds a desired final design thickness of said low-k dielectric layer.

5. The method of claim 4, wherein converting said upper portion is continued until the thickness of said low-k dielectric layer substantially corresponds to said design thickness.

6. The method of claim 1, further comprising heat treating said substrate prior to converting said upper portion of said low-k dielectric layer to promote out-gassing of volatile materials.

7. The method of claim 1, further comprising forming a first resist mask over said sacrificial cap layer and etching a via opening through said sacrificial cap layer and said low-k dielectric layer, wherein resist contamination of said first resist mask is maintained below a specified level.

8. The method of claim 7, further comprising forming a second resist mask over said sacrificial cap layer and patterning an upper portion of said low-k dielectric layer to form a trench over said via opening, the trench having a greater lateral dimension than said via opening.

9. The method of claim 7, further comprising determining a contamination level of photoresist prior to forming said first resist mask.

10. The method of claim 9, further comprising heat treating said substrate to further out-gas said volatile material through said sacrificial cap layer when said determined contamination level exceeds a predefined level.

11. A method, comprising:

forming a silicon-based low-k dielectric layer over a substrate; and

forming a silicon dioxide layer as a sacrificial cap layer on said low-k dielectric layer, wherein volatile materials out-gas from said low-k dielectric layer prior to and during the formation of said silicon dioxide layer.

12. The method of claim 11, wherein forming said silicon dioxide layer includes converting an upper portion of said low-k dielectric layer into low-density silicon dioxide.

13. The method of claim 12, wherein said upper portion is converted into silicon dioxide by exposing said substrate to an oxidizing plasma ambient.

14. The method of claim 11, wherein said low-k dielectric layer is formed with a thickness that exceeds a desired final design thickness of said low-k dielectric layer.

15. The method of claims 2 and 4, wherein converting said upper portion is continued until the thickness of said low-k dielectric layer substantially corresponds to said design thickness.

16. The method of claim 11, further comprising heat treating said substrate prior to forming said silicon dioxide layer to promote out-gassing of said volatile materials.

17. The method of claim 11, further comprising forming a first resist mask over said sacrificial cap layer and etching an opening through said sacrificial cap layer and said low-k dielectric layer, wherein resist contamination of said resist mask is maintained below a specified level.

18. The method of claim 17, further comprising forming a second resist mask over said sacrificial cap layer and patterning an upper portion of said low-k dielectric layer to form a trench over said via opening, said trench having a greater lateral dimension than said via opening.

19. The method of claim 17, further comprising determining a contamination level of photoresist prior to forming said first resist mask.

20. The method of claim 19, further comprising heat treating said substrate to further out-gas said volatile material through said sacrificial cap layer when said determined contamination level exceeds a predefined level.